REMARKS

Claims 1-23 are pending in the present application. Claims 1-5 are currently being considered, and Claim 1 is the sole independent claim currently being considered. Claims 6-23 have been withdrawn from consideration. The Applicant has carefully and thoughtfully considered the Office Action and the comments therein. For the reasons given below, it is submitted that this application is in condition for allowance.

Rejection under 35 U.S.C. § 103(a) over Jahnke in view of Spencer

On pages 2-3, the Office Action rejected claims 1-2 under 35 U.S.C. § 103(a) as allegedly being rendered obvious by Jahnke et al. (U.S. Patent Application Publication No. 2002/0062408) (hereinafter Jahnke) in view of Spencer (U.S. Patent Application Publication No. 2004/0243739) (hereinafter Spencer). Based on the following remarks, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

In rejecting claim 1, the Office Action asserted that Jahnke teaches an apparatus comprising: a direct memory access register adapted to hold a descriptor, said register comprising: a command register comprising a branch enable bit; a source address register; a target address register; and a descriptor address register. To overcome the deficiencies of Jahnke, the Office Action relied upon the teachings of Spencer. According to the Office Action, Spencer teaches in an analogous apparatus wherein a direct memory access register comprises a command register comprising a compare enable bit.

As *amended*, Claim 1 recites an apparatus comprising: a direct memory access register adapted to hold a descriptor, said register comprising: a command register comprising a compare

enable bit and a **single** branch enable bit; a source address register; a target address register; and a descriptor address register. The combination of Jahnke with Spencer fails to teach at least several limitations of amended claim 1 for the following reason.

The combination of Jahnke with Spencer fails to teach a command register comprising a single branch enable bit. The CNTVAL counter 333 of Jahnke uses 16 bits, whereas the command register in amended claim 1 uses a single branch enable bit. Jahnke paragraph [0047] and [0048]. In Jahnke, the CNTVAL counter 333 must be decreased in increments of one to hexadecimal zero (i.e., 0x0000) for the branch to be enabled. Jahnke paragraph [0047] and [0048]. The fundamental difference between a hexadecimal number (a.k.a. a base-16 number) and a decimal number (a.k.a. a base-10 number) is that a hexadecimal number uses 16 instead of 10 as its base for representing digits. A hexadecimal number uses the digits 0 through 9 and the letters A through F to represent the decimal numbers 0 to 15. In a counter implementation of a hexadecimal counter, one hexadecimal number is equivalent to 4 bits. In Jahnke the CNTVAL counter 333 uses 4 hexadecimal digits, which corresponds to 16 bits (4 hexadecimal digits × 4 bits/hexadecimal digit). Hence, Jahnke does not teach the use of a single branch enable bit as receited in amended claim 1.

Therefore, because the combination of Jahnke and Spencer does not teach the recited features of claim 1, it is respectfully submitted that claim 1 is allowable.

Claims 2-5 depend from claim 1, and are allowable as being dependent from an allowable claim.

Conclusion

In light of the above amendments and arguments, it is submitted that claims 9-23 are allowable. Withdrawal of the rejections and a Notice of Allowance are respectfully requested.

Respectfully submitted,

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